# 360-nm SOI process development for high-T applications in harsh environments

Edval J. P. Santos, Senior Member, IEEE, Henrique M. Vasconcelos, Member, IEEE,
Laboratory for Devices and Nanostructures - LDN/NE$^2$N, Universidade Federal de Pernambuco
50740-530, Recife, PE, Brasil. Email: edval@ee.ufpe.br

***Abstract*—Silicon-On-Insulator, SOI, is specially suited for radiation-hard, high-temperature, and high-frequency circuitry. The development of a 360-nm SOI fabrication process is presented. The minimum feature size is selected, as a compromise between ease of fabrication and to allow for the fabrication of RF circuits. The process flow, mask design, lithography, and dimensional characterization results are discussed. The target substrate is an SOI wafer with high resistivity base wafer. For the process development, e-beam lithography is used in all lithographic steps for flexibility. PMMA is used as positive resist, and SU-8 is used as negative resist. The die size is 500 $\mu$m $\times$ 500 $\mu$m. An EKV 2.6 MOSFET model for the developed process was created. The target is the fabrication of 3D integrated smart sensor for harsh environments, such as: on-engine, wheel mounted, and oil & gas production.**

***Keywords*—SOI, harsh environment, process flow**

## I. Introduction

Environment under high-temperature requires special circuit technology. A candidate technology is Silicon-On-Insulator, SOI, which can operate at temperatures as high as 300 $^o$C. High-temperature is one example of harsh ambient condition, other harsh conditions are: humidity, high pressure, radiation, aggressive gases, salty water. Harsh environments are found in the oil & gas industry, chemical plants, food industry, mining, aerospace, car engine, among others. Thus, high-temperature SOI, combined with special packaging, is a technology with high commercial impact in applications which custom design and fabrication can be a competitive advantage. SOI has lower parasitic capacitance, radiation hardness, reduced latch-up, and lower leakage current. Thus being well suited for low-power, low-voltage, high-frequency circuits. Although, it presents lower thermal conductivity due to the insulating layer, which may cause self-heating. SOI-based silicon technology displays high-performance at a competitive cost. Despite the debate, the advantages are such that it has attracted a great deal of interest over the last 35 years, since the development of SIMOX in 1978 [1], [2], [3], [4], [5], [6], [7], [8].

SOI technology has been under development in many research institutes and companies. One such institute is Université Catholique in Louvain-La-Neuve, Belgium [9]. Another example is Fraunhofer IMS in Duisburg, Germany. At Fraunhofer, a 200-mm wafer CMOS-process for high-temperature SOI is available. The feature size can be as low as 0.35 $\mu$m, and the circuits can operate at temperatures as high as 250 $^o$C. The metalization has up to four layers of tungsten, and gold can be deposited onto the pads [10].

Since 2012, the European Union is funding the SOI high-temperature sensing, SOI-HITS, project under the Seventh Framework Program (FP7 ICT) to create integrated smart sensor in SOI technology to measure multiple quantities under temperatures up to 225 $^o$C. The consortium members are: Microsemi, CCMOSS, Cambridge University, Cissoid, Honeywell, IREC, Université Catholique Louvain-La-Neuve, and Warwick University [11].

In this work, a 360-nm SOI process flow, mask design and lithography are presented. The target is the fabrication of 3D integrated smart sensor for harsh environments. such as: on-engine, wheel mounted, and oil & gas production. For the process development, the lithography is carried out with e-beam. Two different e-beam resists were selected: polymethyl methacrylate, PMMA, and epoxy-based, SU-8. PMMA is a positive e-beam resist. SU-8 is a negative photoresist very much used for MEMS applications, as it yields thick layers with vertical sidewalls. It has also been demonstrated that it can be used as a negative e-beam resist [12], [13], [14]. Another application of SU-8, as an e-beam resist, is in the fabrication of refractive optical elements [15]. Another option, as negative e-beam resist, is hydrogen silesquioxane, HSQ. The paper is divided into four sections, this introduction is the first. Next, the methodology is presented. Thirdly, the discussion, and finally the conclusions.

## II. Methodology

In this section, the process flow, mask design, fabrication process, and characterization results are presented. The process under development can use different types of SOI substrates. Thus allowing for processing of different types of circuitry for 3D integration. Types of dice are: analog or RF for transducer signal conditioning, digital for data processing, analog or RF for data communication, analog for energy harvesting, and digital for energy management. As an intermediate step, prior to carrying out full 3D integration, one can build a multi-chip module. In this case, one can use alumina or $Si_3N_4$ ceramic substrates [6]. For this development, the target substrate is smart-cut Wave SOI wafer from SOITEC® with high resistivity base wafer. The specifications are presented in Table I.

### A. Process flow

Considering a Lightly Doped Drain (LDD) MOSFET with polysilicon gate, silicon dioxide insulating layer, two-metal process, plus a high-resistivity (HR) layer, the simplified processing steps are as follows:

Table I. PRIME WAFER SPECIFICATIONS.

| Parameter | Specification |
|---|---|
| Wafer orientation | (100) |
| Wafer diameter | 200 mm (prime) |
| Top silicon thickness | 200 nm |
| Top silicon doping type | P |
| Top silicon resistivity | 20 Ohm.cm |
| Buried oxide thickness (BOX) | 1000 nm |
| Base wafer doping type | P |
| Base silicon resistivity | 1000 Ohm.cm |
| Base wafer thickness | 525 $\mu$m |
| Polish | Double side polish |
| Uniformity | $\pm$ 12.5 nm |

1) Wafer cleaning.
2) Island isolation lithography (mask 1).
3) Silicon etch.
4) Gate oxidation.
5) P-type island implant (mask 2).
6) N-type island implant (mask 3).
7) Polysilicon deposition.
8) Polysilicon lithography (mask 4).
9) Polysilicon etch.
10) Oxide etch.
11) Polysilicon oxidation.
12) Silicon nitride deposition (CVD).
13) LDD spacer lithography (mask 5).
14) LDD spacer etch (RIE).
15) N-type drain/source lithography (mask 6).
16) N-type ion implantation.
17) P-type drain/source lithography (mask 7).
18) P-type ion implantation.
19) Field oxide deposition.
20) Via lithography (mask 8).
21) Oxide etch.
22) Titanium plug formation.
23) Tungsten/Titanium deposition .
24) Metal 1 lithography (mask 9).
25) Metal 1 etching.
26) Field oxide deposition.
27) Via lithography (mask 10).
28) Oxide etch.
29) Titanium plug formation.
30) High-resistivity polysilicon.
31) Polysilicon lithography (mask 11).
32) Polysilicon etch.
33) Field oxide deposition.
34) Via lithography (mask 12).
35) Oxide etch.
36) Titanium plug formation.
37) Tungsten/Titanium deposition.
38) Metal 2 lithography (mask 13).
39) Metal 2 etching.
40) Silicon nitride deposition.
41) Pad lithography (mask 14).
42) Silicon nitride etching.
43) Gold deposition.
44) Gold lithography (mask 15).
45) Gold etching.

The process flow was modeled with IntelliFAB® [16], see Figure 1. At this development stage, planarization has not been applied.

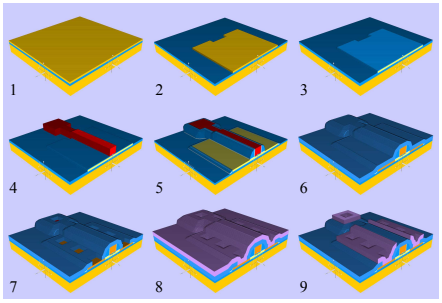


Figure 1. Initial steps of the SOI process flow for MOSFET fabrication, as modeled in Intelifab. 1- wafer cleaning. 2- island lithography, and silicon etch. 3- gate oxidation. 4- polysilicon lithography and etch. 5- lateral spacer formation. 6- field oxide deposition. 7- via lithography and etch. 8- metal deposition. 9- metal lithography and etch.

### B. Mask design

The die area is 500 $\mu$m $\times$ 500 $\mu$m. The test structures are based on the 1.5 $\mu$m-SOI process developed at Tyndall National Institute, Cork, Ireland [17]. The masks were initially designed with Mentor® tools, and edited with Klayout [18]. The design contains MOSFET of different sizes and geometries, as presented in Table II (see Figure 2), an inverter (Figure 3), and a pierce oscillator (Figure 4). The full layout is presented in Figure 5. The layout is divided into four quadrants. The top left quadrant contains MOSFET with annular configuration. The top right quadrant contains high-frequency MOSFET. The bottom left quadrant contains MOSFET with different sizes. The bottom right quadrant contains CMOS inverters and Pierce oscillators. For the CMOS inverters, the length is fixed in 500 nm, and the PMOS is three times as large as the NMOS. There are two Pierce oscillators with $L_{Geom}$= 375 nm. The only difference is $M_4$, one is $W_4$= 100 $\mu$m and the other is $W_4$= 50 $\mu$m. After fabrication, the minimum effective gate length is expected to become 360 nm. The minimum feature size is selected, as a compromise between ease of fabrication and to allow for the fabrication of RF circuits.

Table II. TRANSISTOR SIZES. FOR COLUMNS A AND B, $L \leq W$, AND FOR COLUMNS C AND D, $L \geq W$.

| Row # | $W_A$ ($L_A$=2.5 $\mu$m) | $L_B$ ($W_B$=3.75 $\mu$m) | $W_C$ ($L_C$=5 $\mu$m) | $L_D$ ($W_D$=500 nm) |
|---|---|---|---|---|
| 1 | 2.5 $\mu$m | 375 nm | 0.5 $\mu$m | 0.5 $\mu$m |
| 2 | 5.0 $\mu$m | 500 nm | 1.0 $\mu$m | 1.0 $\mu$m |
| 3 | 7.5 $\mu$m | 625 nm | 1.5 $\mu$m | 1.5 $\mu$m |
| 4 | 10.0 $\mu$m | 750 nm | 2.0 $\mu$m | 2.0 $\mu$m |

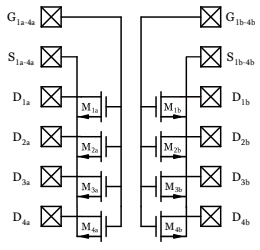


Figure 2. MOSFET with different sizes.

### C. Fabrication process

The fabrication procedure was carried out at the Laboratory for Devices and Nanostructures (LDN/NE$^2$N/UFPE) clean

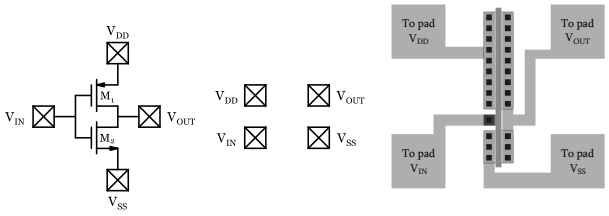


Figure 3. Digital test block is an inverter. On the right, the layout.

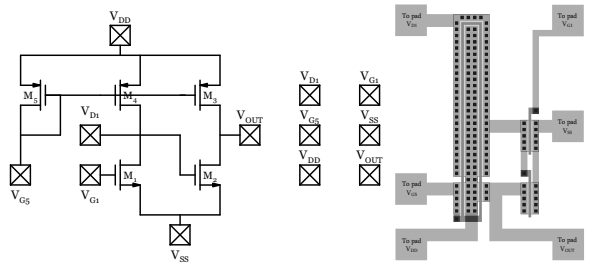


Figure 4. Analog test circuit is a Pierce oscillator block. Layout on the right.

room. For the lithography development step, SOI monitor wafers from SOITEC are used. The monitor wafer has 10000-nm thick buried oxide, and 3400-nm thick top silicon layer. The wafer is diced into smaller pieces for process development. Four masks were selected for the initial process development, as presented in Table IV, and e-beam lithography is used in all lithographic steps for flexibility. Although, a mix-and-match process is considered, as a mask aligner (EVG-620) with submicron capability is available in the clean room.

*1) E-beam lithography:* The lithography system is an JEOL 6460® scanning electron microscope with an NPGS® control board. The designed structures are transferred to the e-beam lithography computer as GDS files. After reading into the NPGS system, run files are generated for exposure. Two different resists are used, as shown in Table IV. The positive resist is PMMA (ARP 651-09-496k), and the negative resist is SU-8 2. Both resists were diluted in thinner 1:2 [19], [20].

The substrate is initially dipped into Piranha etch ($H_2SO_4$:$H_2O_2$), rinsed in de-ionized (DI) water, BOE, and DI water. After spin dry, it is baked at 200 $^oC$ for 10 min. Next, the substrate is spin coated at 4000 rpm for 30 s. For PMMA, the pre-bake temperature is 150 $^oC$ for 20 min. For SU-8 2, the pre-bake is a two-step process, 65 $^oC$ for 60 s, and 95 $^oC$ for

Table III. CMOS INVERTER WITH L= 500 NM.

| Row # | Type | W |
|---|---|---|
| 1,2 | NMOS | 2 $\mu$m |
| | PMOS | 6 $\mu$m |
| 3 | NMOS | 3 $\mu$m |
| | PMOS | 9 $\mu$m |

Table IV. SELECTED MASKS FOR PROCESS DEVELOPMENT.

| Mask # | Description | E-beam resist type |
|---|---|---|
| 1 | Island isolation | Negative |
| 4 | Polysilicon | Negative |
| 8 | Via | Positive |
| 9 | Metal | Negative |

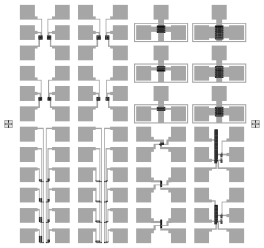

Figure 5. Die with 500 $\mu$m $\times$ 500 $\mu$m. The top left quadrant has MOSFET with annular configuration. The top right quadrant has high-frequency MOSFET. The bottom left quadrant has MOSFET with different sizes. The bottom right quadrant has CMOS inverters and Pierce oscillators.

60 s. The exposure is carried out at 30 KV. The SEM control is carried out over EDSI with PG_EDSI. Typically, the beam current is set in the 2.5 pA to 10 pA range. The maximum useful beam current is 1 nA.

For mask #8 (see Table IV), PMMA is exposed with a line dose of 1.3 $\mu$C/cm. Post-baked at 100 $^oC$ for 60 s.

After exposure, the wafer is developed in methyl isobutyl ketone, MIBK, mixed with isopropyl alcohol, IPA, 1:1, for 60 s. IPA (or AR 600-60) is also used as stopper, dip in IPA for 30 s.

For masks #1, #4, and #9 (see Table IV), SU-8 2 is used. The area dose is 0.8 $\mu$/cm$^2$. After exposure, a post exposure bake is required to cross-link the exposed areas. This is performed in two steps: 65 $^oC$ for 60 s, and 95 $^oC$ for 60 s. Next, the wafer is developed by immersion with SU-8 developer for 60 s. Finally, the substrate is rinsed in isopropyl alcohol.

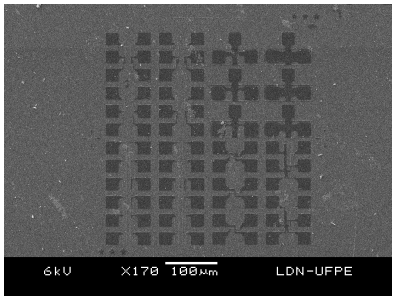


Figure 6. E-beam lithography of metal layer to demonstrate SU-8 2 as negative resist.

*2) Metalization:* Tungsten metalization is carried out in an ultra-high vacuum sputtering system (ATC Orion, AJA international) under argon plasma. The gold layer metalization is deposited in a thermal evaporator (Auto 306, Edwards).

*3) Dielectric layer:* Silicon oxide layer deposition is carried out in an ultra-high vacuum sputtering system (ATC Orion, AJA international) under argon plasma and a silicon dioxide target. For the silicon nitride layer, a mixture or argon and nitrogen plasma is generated, as a silicon target is used.

### *D. Characterization*

Dimensional characterization is performed with a scanning electron microscope (JEOL 6460). See Figure 7.

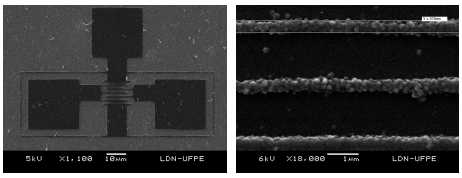

Figure 7. Left: interdigitated MOSFET. Right: polysilicon layer.

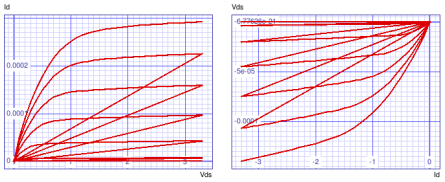

Figure 8. Expected NMOS and PMOS low-frequency $I_D \times V_{DS}$ curves, as traced in SPICE Opus with an EKV 2.6 model for the proposed fabrication process.

## III. Discussion

The use of e-beam lithography has allowed for fast process prototyping. The combination of positive and negative e-beam resists reduces exposure times. In this report, PMMA, as a positive resist, is used for the via lithography steps. SU-8 was selected as the negative resist, as it offers a wide range of thicknesses. SU-8 is used for the island isolation, polysilicon, and metal layers. The exposure was carried out with NPGS v9.0, which has a nominal resolution of $1/2^{16}$, as it uses 16-bit DAC. However, this ultimate resolution is not achieved. In practical settings, the thinnest line is about $1/2000$ of field side. For $500 - \mu m$ field side, used in this work, implies a $250 - nm$ resolution, which is good enough for the target process. Although, a mix-and-match approach can be applied. Thus allowing a higher current, further reducing exposure times.

In Figure 6, a die exposed with SU-8 is presented. The die area is $500\,\mu$m $\times$ $500\,\mu$m. Different devices and circuits are designed in this die. For the metalization lithography level, it is observed that the presence of the metal layer reduces proximity effects.

For the proposed process, the expected device model was developed in EKV 2.6. The low-frequency $I_D \times V_{DS}$ curves in SpiceOpus [21] are presented in Figure 8. The oxide thickness is 10 nm, NMOS threshold voltage is 0.5 V, and PMOS threshold voltage is -0.5 V. Voltage level is 3.3 V.

## IV. Conclusion

High-temperature SOI has a great potential for application in harsh environments. The process under development combines SOI active devices with tungsten metal layers to fabricate reliable integrated circuits. Wafer selection, mask design, and e-beam lithography for the development of an 360-nm SOI process with die size of $500\,\mu$m$\times 500\,\mu$m were discussed. In particular, four lithography steps were presented in this paper, namely: island isolation, polysilicon, via, and metal. For the via lithography, PMMA is used. For the other three layers, SU-8 2 is used. The combination of PMMA and SU-8, as positive, and negative e-beam resists, respectively, is a feature of this process development.

The expected device parameters were used to generate an EKV v2.6 model. The approximate device parameters were used in SPICE Opus, level 44, to trace the NMOS and PMOS low-frequency $I_D \times V_{DS}$ curves.

The target of this development is the fabrication of 3D integrated smart sensor for harsh environments. Next, silicon etch for thru-wafer vias, and MOSFET fabrication will be addressed. This effort can also be used to train process engineers.

## Acknowledgment

The authors are thankful to the Tyndall Institute (Cork, Ireland), specially Eng. Carlo Webster, and Eng. Brendan O'Neill, PETROBRAS oil company, FINEP, and CNPq. The authors are thankful to Eng. Mauricio Galassi from PETROBRAS for valuable discussions on the oil well environment.

## References

[1] J.-P. Colinge, Silicon-on-Insulator technology: materials to VLSI. Springer Verlag (1991), 3rd ed. Kluwer (2004).

[2] Y. Arimoto, High-temperature operation of NMOSFET on bonded SOI, IEICE Trans. on Electronics, **E75C**/12, 1442-1446 (1992).

[3] D. Flandre, A. Terao, P. Francis, B. Gentinne, J.-P. Colinge, Demonstration of the potential accumulation-mode MOS-transistors on SOI substrates for high-temperature operation (150-300 $^o$C), IEEE Electron Dev. Lett., **14**, 10-12 (1993).

[4] R. R. Grzybowski, S. M. Tyson, High-temperature testing of SOI devices to 400 $^o$C, 1993 IEEE International SOI Conference Proceedings, 176-177 (1993).

[5] G.-S. Chung, Thin SOI structures for sensing and integrated circuit applications, Sensors and Actuators A: Physical, **39**, 241-251 (1993).

[6] P. Hagler, P. Henson, R. Wayne-Johnson, Packaging technology for electronic applications in harsh high-temperature environments, IEEE Trans. on Industrial Electronics, **58**, 2673-2682 (2011).

[7] L. Toygur, A. C. Patil, J. Guo, X. Yu, S. L. Garverick, A 300 $^o$C, SOI transimpedance amplifier with application to capacitive temperature sensing, IEEE Sensors 2012, Taipei, 28-31 Oct. 2012.

[8] M. Emam, J.-P. Raskin, Partially depleted SOI versus deep N-well protected bulk-Si MOSFETs: a high-temperature RF study for low-voltage low-power applications, IEEE Trans. on Microwave Theory and Techniques, **61**, 1496-1504 (2013).

[9] http://www.uclouvain.be/en-352440.html

[10] http://www.ims.fraunhofer.de

[11] http://www.soi-hits.eu/

[12] B. Bilenberg, S. Jacobsen, M. S. Schmidt, L. H. D. Skjolding, P. Shi, P. Bøggild, J. O. Tgenfeldt, A. Kristensen, High resolution 100 kV electron beam lithography in SU-8, Microelectronic Engineering, **83**, 1609-1612 (2006).

[13] A. K. Nallani, W. S. Park, J. B. Lee, Characterization of SU-8 as a photoresist for electron-beam lithography. Smart Sensors, Actuators, and MEMS. Edited by J.-C. Chiao, V. K. Varadan, C. Cane. Proceedings of the SPIE, **5116**, 414-423 (2003).

[14] F. Williamson, E. A. Shields, SU-8 as an electron beam lithography resist, Proceedings of the 15th Biennial University/Government/Industry Microelectronics Symposium, 2003.

[15] E. A. Shields, F. Williamson, J. R. Leger, Electron-beam lithography for thick refractive optical elements in SU-8, J. of Vac. Sci. & Tech. B, **21**, 1453-1458 (2003).

[16] http://www.intellisense.com/

[17] http://www.tyndall.ie/

[18] http://www.klayout.de/

[19] http://www.microchem.com/

[20] M. Shaw, Epoxy Business Unit - Sales and Technical Support Manager MicroChem Corp.

[21] http://www.spiceopus.si/